

**REMARKS**

Several claim amendments have been presented herein, and several new claims have been added, in order to more clearly delineate the scope of Applicant's invention. Applicant respectfully requests entry of the foregoing amendment prior to examination.

Respectfully submitted,

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**ATTACHMENT TO PRELIMINARY AMENDMENT -  
VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

1. (Amended) A method for improving the performance of an RF power amplifier circuit comprising:  
sensing [the] a collector current in [the] an input stage transistor;  
feeding [said current to the] a current equal or proportional to said input stage transistor collector current to an output stage bias circuit to boost the [output] bias of an output stage;  
wherein the input stage transistor is operated in a class AB mode, and said output stage is fed through a matching network.
2. (Amended) The method of claim 1, wherein the input stage transistor collector current is sensed and fed to the output stage bias circuit via a current mirror.
3. (Amended) The method of claim 2, [where the current at the entry terminal of the input stage transistor is the mirrored current] wherein one transistor comprising said current mirror is connected in series with a transistor that itself forms a second current mirror with the input stage transistor.
4. (Amended) The method of [any of claims 1-3] claim 3, wherein the amplifier circuit comprises plural bipolar junction transistors (BJTs).
5. (Amended) The method of [any of claims 1-3] claim 3, wherein the amplifier circuit comprises plural field effect transistors (FETs).
6. (Amended) The method of [any of claims 1-3] claim 3, wherein the amplifier circuit comprises a combination of BJTs and FETs.
7. (Amended) A transistor circuit, comprising:

an input stage;

an output stage with a biasing circuit; and

a current mirror, which senses [the] an input signal current and feeds [it] a current proportional to said input signal current to [the] an output stage biasing circuit.

8. (Amended) The circuit of claim 7, [where the circuit comprises] wherein said current mirror includes as least one BJT[s].
9. (Amended) The circuit of claim 7, [where the circuit comprises] wherein said current mirror includes as least one FET[s].
10. (Amended) The circuit of claim 7, [where the circuit comprises a combination of] wherein transistors comprised within said circuit include both BJTs and FETs.
11. (Amended) A method of adaptively boosting the output stage bias of an amplifier circuit, comprising:

sensing [the] an input signal; and

boosting [the] an output stage bias with a current equal or proportional to the input signal.
12. The method of claim 11, where the input signal is an RF signal.
13. (Amended) The method of claim 12, where the input signal is sensed by a current mirror [biasing circuit for the input stage].
14. (Amended) The method of claim 13, where [the] a collector current of an input stage BJT is mirrored by the current mirror and fed into an output stage biasing circuit.
15. (Amended) The method of claim 13, where [the] a drain current of an input stage FET is mirrored by the current mirror and fed into an output stage biasing circuit.

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16. (Amended) The method of [any of claims 13-15] claim 15, where the current mirror comprises BJTs.
17. (Amended) The method of [any of claims 13-15] claim 15, where the current mirror comprises FETs.
18. (Amended) A subcircuit, to be used in an amplification circuit, comprising:  
an input sensor, arranged to sense [the] an input signal to the amplification circuit;  
and  
an output stage booster, arranged to boost a bias of an output stage of the  
amplification circuit in proportion to said input signal.
19. The subcircuit of claim 18, where the input signal is an RF signal.
20. (Amended) The subcircuit of [either of claims 18 or 19] claim 19, where the input sensor is a current mirror.

Claims 21-26 are new.